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| **Course Name:** | **Hardware Description Language Lab (2UXL401)** | **Semester:** | **IV** |
| **Date of Performance:** | **12/01/2021** | **Batch No:** | **B2** |
| **Faculty Name:** | **Prof. Bhargavi Kaslikar** | **Roll No:** | **1912052** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** |  |

**Experiment No: 1**

**Title:** Study of basic VHDL code: Adder (Dataflow)

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| **Aim and Objective of the Experiment:** |
| Write a VHDL code   1. To implement a half adder. 2. A full adder using half adder 3. A 4-bit adder using full adder.   Write a testbench to verify your results for half adder and four bit adder Implement the full adder on CPLD.  To study basic structure of VHDL code and to understand use of test bench for simulation.  To know the process for implementation on CPLD. |

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| **COs to be achieved:** |
| **CO 1**: Use basic Concurrent and Sequential statements in VHDL and write codes for simple applications  **CO 2**: Test a VHDL code and verify the circuit model.  **CO 3**: Synthesize and Implement the designed circuits on CPLD/ FPGA. |

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| **Work to be done** |
| Upload VHDL codes for half adder, full adder ( structural) and four-bit adder (structural) and test bench for half adder and 4-bit adder.  Also Upload Simulation waveforms for 4 bit adder.  Upload scanned image for post lab questions  **Half Adder:**    Entity – half-adder:    Testbench – Half-adder:      Waveform – Half-adder:    Full Adder:    Entity – Full-adder:    Testbench – Full-adder:      Waveform – Full-adder:    **4-bit Adder using Full-adder:**    Entity – 4-bit adder:      Testbench – 4-bit adder:      Waveform – 4-bit adder: |

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| **Post Lab Subjective/Objective type Questions:** |
| Upload Answer of following question before coming to next laboratory.  Q1. **Analyse the following code and write its output.**  library ieee;  use ieee.std\_logic\_1164.all;  entity xyz is  port ( x,y: in std\_logic;  z : out std\_logic);  end entity;  architecture arch\_xyz of xyz is  begin  z <= '0' when (x=’1' and y='1') else  '0'when (x='0' and y='0')else  '1';  end arch\_xyz;  Ans:  The given code is similar to XOR gate as the output ‘z’ is low (0) if both the inputs ‘x’ and ‘y’ are same i.e. if both of them are high or if both of them are low at the same time. Output is high if ‘x’ and ‘y’ are different.   |  |  |  | | --- | --- | --- | | x | y | **z** | | 0 | 0 | **0** | | 0 | 1 | **1** | | 1 | 0 | **1** | | 1 | 1 | **0** |   **Q 2 Write a test bench for the above code**  **Ans:** |

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| **Conclusion:**  We studied the basics VHDL coding.And implemented Half adder Full adder and 4bit adder |

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| **Signature of faculty in-charge with Date:** |